CLAIMS:

1. A method for interference compensation in a phase-locked loop comprising a voltage-controlled frequency generator, wherein the frequency generator is tuned to a nominal frequency via a tuning voltage V_{tune} and whose actual frequency is compared with a reference frequency by means of a frequency comparison and is tuned if a deviation is discovered via the frequency comparison, in which method in the event of interference the tuning voltage V_{tune} is changed by an interference voltage $V_{stör}$ that depends on the interference event and thus a frequency deviating from the nominal frequency is generated, which is corrected again by the phase-locked loop, characterized in that if a known interference event occurs, a voltage V_{comp} which compensates for the interference voltage $V_{stör}$ is generated in synchronism with this with sign inversion and is superimposed on the interference voltage $V_{stör}$.

2. A method as claimed in claim 1, characterized in that the relevant associated compensation voltage V_{comp} is determined in a measuring operation for all the possible known interference events, and that this is stored in a compensation table.

3. A method as claimed in claim 2, characterized in that the measuring operation and the storage of the voltage values in the compensation table take place when the arrangement is made operative and/or during operation.

4. A method as claimed in claim 1, characterized in that the relevant compensation voltage value which is saved in the compensation table is read out prior to a known interference event, which event causes interference voltage $V_{stör}$ to occur, and with this compensation voltage value the compensation voltage V_{comp} is controlled in synchronism with the occurrence of the interference voltage.

5. An arrangement for interference compensation in a phase-locked loop comprising a voltage-controlled frequency generator, wherein the frequency generator has a V_{tune} input and a VarGND terminal, characterized in that the VarGND terminal for the voltage-controlled frequency generator (3) is connected to a controllable voltage source.

6. An arrangement as claimed in claim 5, characterized in that the controllable voltage source comprises a resistor connected between the VarGND terminal and the GND potential and a controllable current source connected between the VarGND terminal and the resistor.

7. An arrangement as claimed in claim 6, characterized in that the VarGND terminal of the voltage-controlled frequency generator (3) is connected to a digital-to-analog converter (5) which generates a compensation current, and in that the digital-to-analog converter (5) is connected to two registers via a transmit/receive change-over switch.

8. An arrangement as claimed in claim 5, characterized in that the VarGND terminal is connected to the controllable voltage source via a voltage divider in such a way that the voltage divider is connected via a first partial resistor to the controllable voltage source, and the second partial resistor, which is connected in series, is connected to the GND potential and the VarGND terminal with the connection to the first partial resistor is connected to the second partial resistor.

9. An arrangement as claimed in any one of claims 5 to 8, characterized in that a phase detector charge pump (1) is arranged to which a reference clock is applied via a first phase detector input (PDin1), wherein the output of the phase detector charge pump (Cpout) is connected to the input of a voltage-controlled frequency generator (3) via a loop filter (2), wherein the output of the voltage-controlled frequency generator (3) is connected to a second phase detector (PDin2) via a frequency divider (4), wherein, furthermore, a measuring circuit is arranged, and wherein the loop filter (2) comprises a first capacitor at the input end, a third capacitor at the output end, a second resistor arranged between the input and the output of the loop filter and a series circuit which is connected to the input and comprises a first resistor and a second capacitor, wherein the second capacitor of the series circuit is connected to the input of the measuring circuit, while the input in the measuring circuit forms a virtual ground terminal.

10. An arrangement as claimed in claim 9, characterized in that the measuring circuit comprises a negative-feedback inverting operational amplifier arrangement (6) and an analog-to-digital converter unit (7).

11. An arrangement as claimed in any one of claims 5 to 8, characterized in that a measuring circuit is connected to the V_{tune} input of the voltage-controlled frequency generator (3), that the measuring circuit comprises a first operational amplifier which works as a buffer amplifier whose output is connected via a first resistor and a capacitor to the inverting input of a second operational amplifier, working as a negative-feedback inverting amplifier, that the non-inverting input of the second operational amplifier is connected to a reference voltage, that the output of the second operational amplifier is fed back to the inverting input via two anti-parallel diodes, that the output of the second operational amplifier is further connected via a second resistor to the connection of the first resistor and the capacitor, and the output of the second operational amplifier has a TDet terminal for outputting a voltage.